REAL TRANSPORT DOCKET NO.: 240438US2/ele

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:

GROUP: 2812

Hirokazu SAYAMA, et al.

SERIAL NO: 10/620,379

ATTENTION:

FILING RECEIPT CORRECTIONS

FILED:

July 17, 2003

FOR:

SEMICONDUCTOR DEVICE INCLUDING GATE ELECTRODE FOR

APPLYING TENSILE STRESS TO SILICON SUBSTRATE, AND METHOD

OF MANUFACTURING THE SAME

## REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

Office of Initial Patent Examination Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

The Patent Office is requested to provide a corrected Official Filing Receipt for the attached. No fees are required. If you have any questions, please do not hesitate to contact us.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C.

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**CONFIRMATION NO. 8754** 

22850 OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET **ALEXANDRIA. VA 22314** 

FILING RECEIPT \*OC000000011070963\*

Date Mailed: 10/21/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an err r is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with th changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

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Type of Resp(s): \_ Due Date(s):

OBLON, SPIVAK, McCLELL

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DOCKETING DEPT

MAIER & NEUSTADT, P.C.

Applicant(s)

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**Assignment For Published Patent Application** 

Renesas Technology Corp., Tokyo, JAPAN;

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2002-336669 11/20/2002

If Required, Foreign Filing License Granted: 10/20/2003

Projected Publication Date: 05/20/2004

N n-Publication Request: No

Early Publication Request: No

Title

Semiconductor device inlcuding gate electrode for applying tensile stress to silicon substrate, and method of manufacturing the same

Pr liminary Class

PLEASE NOTE THAT THE TITLE IS INCORRECT. IT SHOULD READ AS FOLLOWS:

SEMICONDUCTOR DEVICE INCLUDING GATE ELECTRODE FOR APPLYING TENSILE STRESS TO SILICON SUBSTRATE, AND METHOD OF MANUFACTURING THE SAME